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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,523	06/27/2001	Ryan N. Rakvic	2207/1123601	3187

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	14

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/891,523	RAKVIC ET AL.
	Examiner	Art Unit
	Midys Inoa	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-23 and 26-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-23 and 26-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 9-12, 14-23, 26-29, 34, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Rappoport et al. (6,549,987).

Regarding Claims 1, 19 and 29, Rappoport et al. teaches a cache (Figure 3) comprising a plurality of independently addressable cachelets (Figure 3, # 310 and Column 3, lines 51-59), each cachelet ("bank") to provide data responsive to independent load requests in a single clock cycle (Abstract, lines 1-4; it is understood that in order for multiple data items to be retrieved from the cache in a single clock cycle, independent addresses must be received by each bank on the same clock cycle).

Regarding Claim 2, Rappoport discloses a cache, which is a member of a multiple layer cache system (Figure 2, #210 represents one layer and #220 represents a second layer).

Regarding Claim 3, Rappoport discloses an address manager (Figure 4, #460) coupled to an input of the cache (#440) and to each of the cachelets (each access line to coupling the cache directory and the cache represents an access line to each bank).

Regarding Claim 4, Rappoport discloses cachelets comprising a plurality of cache entries (Figure 3, address lines $addr_0$ to $addr_{N-1}$), each cache entry having tag and data fields (Figure 3, "T" and "D"), and address decoder coupled to an address input and to the cache entries(Figure 3, #330) and a tag comparator (Figure 3, #340) coupled to the address input and to the tag fields of the cache entries (See Column 3, lines 37-50).

Regarding Claim 5, Rappoport discloses the address inputs of each of the cachelets being independent from each other ("each cache bank is independently addressed", see Abstract).

Regarding Claims 6 and 7, Rappoport discloses the cache of claim 1 (as discussed above), and instruction decoder (Figure 3, #330), an address manager coupled to the instruction decoder (Figure 4, #460) and a plurality of load units coupled to the address manager (not shown), each of the load units coupled to a respective one of the cachelets. The load units are interpreted to be access circuitry normally used to enable reading and writing ("access mechanism") into a cache memory and such circuitry would normally be located on an interconnect ("access line") between the address manager and each cache bank or cachelet (See Microsoft Computer Dictionary, page 12 for support of the definition of an access mechanism).

Regarding Claims 9-11 and 14, Rappoport discloses a method comprising: receiving plural data requests ("separate address signal for each of the banks", Column 3, lines 51-59), each associated with respective cachelet pointers ("a cache line is typically addressed by a portion of an instruction pointer called a set", Column 3, lines 51-59 and "an instruction segment

and a bank vector identify which of the banks is to be addressed with the set", Column 4, lines 44-60), determining whether any of the cachelet pointers conflict with any other cachelet pointers, if a conflict occurs among cachelet pointers, forwarding one of the data requests associated with a conflicting cachelet pointer to the identified cachelet, and reassigning data requests associated with remaining conflicting cachelet pointers to unused cachelets (Column 5, lines 34-51).

Regarding Claims 12 and 15, Rappoport discloses determining whether any of the cachelet pointers are valid (Column 5, lines 17-33), forwarding data requests having valid, non-conflicting cachelet pointers to the addressed cachelet, and assigning data requests of non-conflicting cachelet pointers to unused cachelets according to a default assignment scheme.

Regarding Claims 16 and 26, Rappoport discloses receiving plural data requests and associated cachelet pointers (Figure 3, $addr_0$ to $addr_{N-1}$ and "set"), the cachelet pointers addressing one of a plurality of cachelets within a cache (Figure 3, "banks" #310), determining whether any of the cachelet pointers are valid, forwarding data requests having valid cachelet pointers to the addressed cachelet, and assigning remaining data requests to unused cachelets according to a default assignment scheme (Column 5, lines 5-33).

Claims 17-18 and 27-28 are rejected with the same rationale as that of claims 9-11.

Regarding Claim 20, Rappoport discloses, the cache system of claim 19 (as discussed above) provided as a first layer cache (cache within a "instruction segment engine"), and a second layer of cache ("instruction cache") to receive a load that misses the cachelet to which it was assigned (data may be loaded into or supplied by either the instruction cache or the cache within the ISE depending of where it is available, Column 3, lines 4-37 and Figure 2).

Regarding Claim 21, the instruction cache #210 of Rappoport can be a system memory (Figure 2).

Regarding Claim 22, Rappoport discloses a first layer cache (Figure 2, #280 and Figure 3) comprising a plurality of independently addressable cachelets (Figure 3, # 310 and Column 3, lines 51-59), and means for distributing multiple loads among the cachelets ("bank") in a single clock cycle ("single clock cycle... independently addressed", see Abstract), and a second layer of cache ("instruction cache", Figure 2, #210) to receive a load that missed the cachelet to which it was assigned (data may be loaded into or supplied by either the instruction cache or the cache within the ISE depending of where it is available, Column 3, lines 4-37 and Figure 2).

Regarding Claims 21 and 23, the instruction cache #210 of Rappoport can be a system memory (Figure 2).

Regarding Claim 34, Rappoport discloses a cache management method, comprising: receiving plural data requests (Figure 3, $addr_0$ to $addr_{N-1}$) and in unison ("single clock cycle", Abstract) directing one data requests to each cachelet within the cache (see Figure 3), for each cachelet, determining if the respective data request hist the cachelet (function of the comparators #340, Figure 3 and Column 3, line 60 – Column 4, line 6) and, if so, performing the respective data request.

Regarding Claim 36, Rappoport discloses a management method which if a respective data request does not hit its cachelet; the data request is directed to another cache layer (data may be loaded into or supplied by either the instruction cache or the cache within the ISE depending of where it is available, Column 3, lines 4-37 and Figure 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13, 30-33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rappoport et al. (6,549,987).

Regarding Claims 13 and 35, Rappoport et al. teaches the invention as set forth by Claims 10 and 34 above. Rappoport et al. does not teach storing copies of a single data item in multiple cachelets ("banks"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to store copies of the same data item in multiple cachelets ("posting a write request simultaneously to all the cachelets") since in a common multiple cache system data that is often stored in more than one cache in order to ensure that a data item is always available when needed.

Regarding Claims 30-33, Rappoport et al. teaches the invention as set forth by Claims 10 and 14 above. Rappoport et al. does not teach forwarding the reassigned data requests in parallel with the other forwarded data requests. It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the invention of Rappoport et al. to forward reassigned commands in parallel to other commands since the system already has the ability to address the memory banks independently from one another during the same clock cycle (in other words, it has the ability to address memory banks in parallel) and extending this parallel ability

to the reassigned requests would allow for these requests to be processed faster and more efficiently.

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

midys Inoa

Midys Inoa
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